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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/810,309 | 03/26/2004 | Isamu Akasaki | 81716.0122 | 8006 |

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| EXAMINER | |
|---|---|
| LE, THAO X | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/810,309 | AKASAKI ET AL. | |
| | Examiner | Art Unit | |
| | Thao X. Le | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2,4,6,8,10-13 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,6,8,10-13 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 31 Mar 2006 has been entered.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 2, 4, 6, 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6583468 to Hori et al (or EP 1213767) in view of US 6586819 to Matsuoka.

Regarding claim 2, Hori discloses a semiconductor apparatus in fig. 3 comprising: a substrate 1 made of a diboride single crystal, column 6 lines 12-13 expressed by a chemical formula $XB_2$, in which X includes at least one of Ti, Zr, Nb and Hf, column 6 line 13; a semiconductor buffer layer 2, column 4 line 67, formed on a principal surface of the substrate 1 and made of $(AlN)_x(GaN)_{1-x}$ ($0 < x \leqq 1$) or AlN when x=1, column 4 line 67, nitride semiconductor layer 3 or 13 formed on the semiconductor buffer layer 2, including at least one kind or plural kinds selected from among 13 group elements and As, column 5 line 2 or col. 7 line 54 (n-GaN).

But Hori does not disclose a semiconductor apparatus wherein an angle θ1, formed by a normal line of a principal surface of the substrate and a normal line of a (0001) plan of the substrate is $0^{\circ} < \theta 1 \leq 0.55^{0}$

However, Matsuoka discloses a semiconductor apparatus wherein an angle θ1 (tilt angle), fig. 3C-D, formed by a normal line of a principal surface of the substrate and a normal line of a (0001) plan of the substrate is $0^{\circ} < \theta 1 \leq 2^{0}$, col. 8 line 38. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the substrate tilt angle teaching of Matsuoka with

Hori's device, because it would have formed a flat surface and good crystallinity as taught by Matsuoka, col. 4 line 9.

Note: 'the 13 group element' is being defined as Group III B comprises Ga, Al, In, H, and Ti.

Regarding claim 4, Hori discloses the semiconductor apparatus of claim 1, wherein the substrate 1 is of $ZrB_2$ or $TiB_2$, column 6 line 13.

Regarding claim 6, Hori discloses Otani discloses the semiconductor apparatus wherein the substrate 1 is a solid solution containing one or a plurality of impurity elements of 5 atom % or less (zero impurity is less than 5), the one or a plurality of impurity elements being selected from a group consisting of Ti, Cr, Hf, V, Ta and Nb when the substrate is of $ZrB_2$.

Regarding claim 8, Hori discloses the semiconductor apparatus of claim 2, wherein the semiconductor buffer layer 2 is AlN, column 4 line 67.

Regarding claim 19, Hori discloses the semiconductor apparatus of claim 2, wherein the substrate is eroded and removed by etching.

The process "eroded" or "etching" in claim 19 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985). In addition, the recitation of 'eroded' or 'etching' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

5. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6583468 to Hori et al. and US 6586819 to Matsuoka and further in view of US 680948 to Koike et al (or EP 1263031).

Regarding claims 10-11, Hori does not the thickness of the semiconductor buffer layer made of AlN is about 10-250 nm or 10-100 nm.

But Hori discloses the semiconductor apparatus of claim 8, wherein the thickness of the semiconductor buffer layer made of AlN is about 500 nm, column 6 line 4. Accordingly, it would have been obvious to one of ordinary skill in art to use the thickness of Hori in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 12-13, Hori does not disclose the semiconductor apparatus of claim 2, wherein x of the semiconductor buffer layer made of $(AlN)_x(GaN)_{1-x}$ is $0.1 \leqq x \leqq 0.1$ or $0.4 \leqq x \leqq 0.6$.

However, Hori discloses the conventional buffer layer 2 is made of GaN having Al element at least 50% atomic percentage, column 5 line 39-46. Furthermore, Koike discloses the buffer layer having the composition of $Al_xGa_{x-1}N$ ($0 \leqq x \leqq 1$), column 8 line 26. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the buffer layer teaching of Koike with Hori's buffer layer, because it would have suppressed generation of

threading dislocation as taught by Koike. In addition, it would have been obvious to one of ordinary skill in art to use the teaching of Koike and Hori in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

The formula $(AlN)_x(GaN)_{1-x}$ is $0.1 \leqq x \leqq 0.1$ or $0.4 \leqq x \leqq 0.6$ is being interpreted as for example when x=0.4, then it would be $Al_{0.4}N_{0.4}Ga_{0.6}N_{0.6}$. Thus, this formula would be chemically equivalent to $Al_{0.4}Ga_{0.6}N$.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
26 April 2006